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FIG. 1A(PRIOR ART)

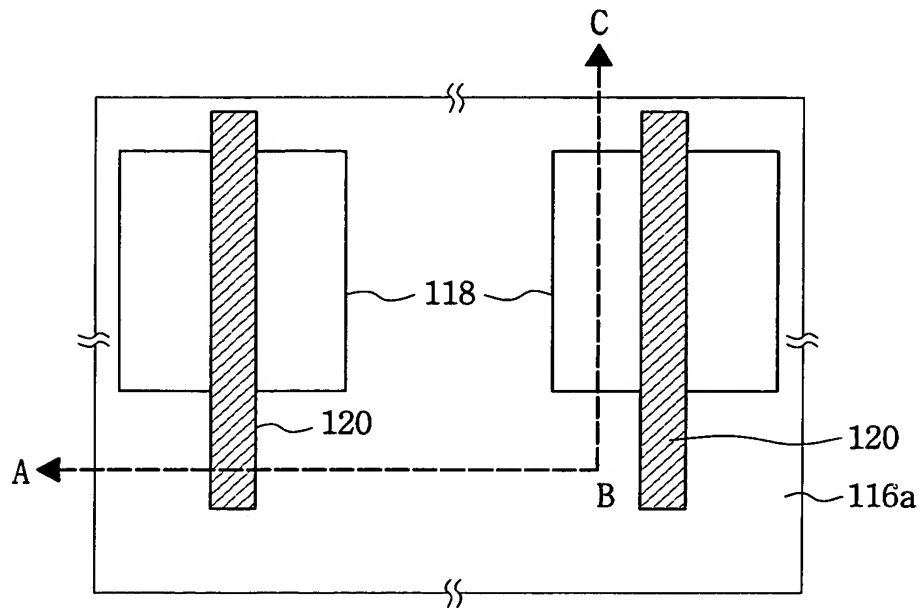


FIG. 1B(PRIOR ART)

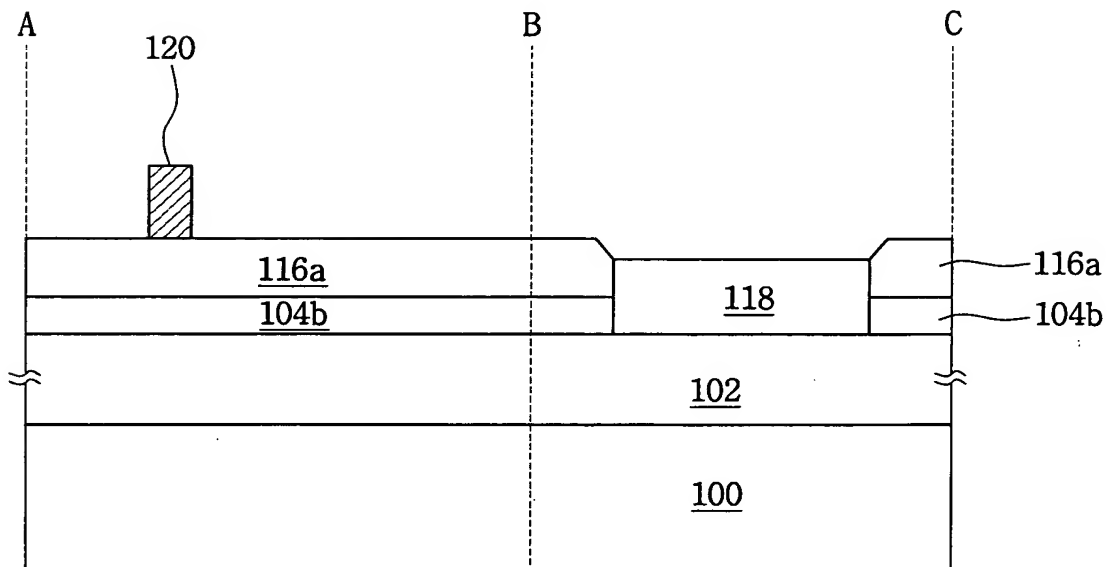




Fig. 1 is a cross-sectional view of a semiconductor device 100. The device 100 includes a substrate 100, a base layer 102, a gate stack 116a, a gate electrode 118, a channel layer 128, a source/drain region 120, and a contact layer 122. The device is divided into regions A, B, and C by dashed lines.

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FIG. 4A

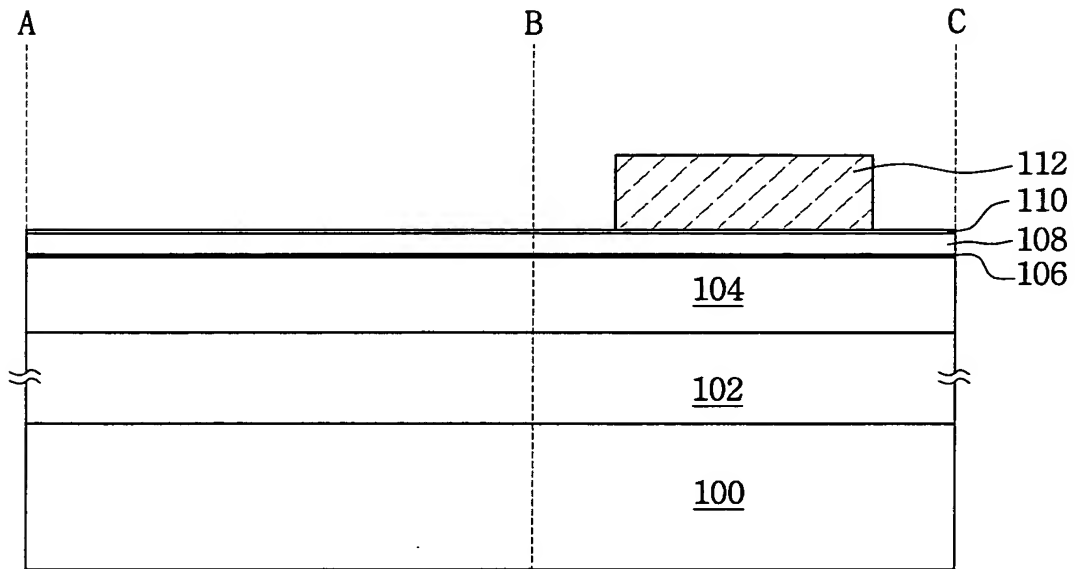
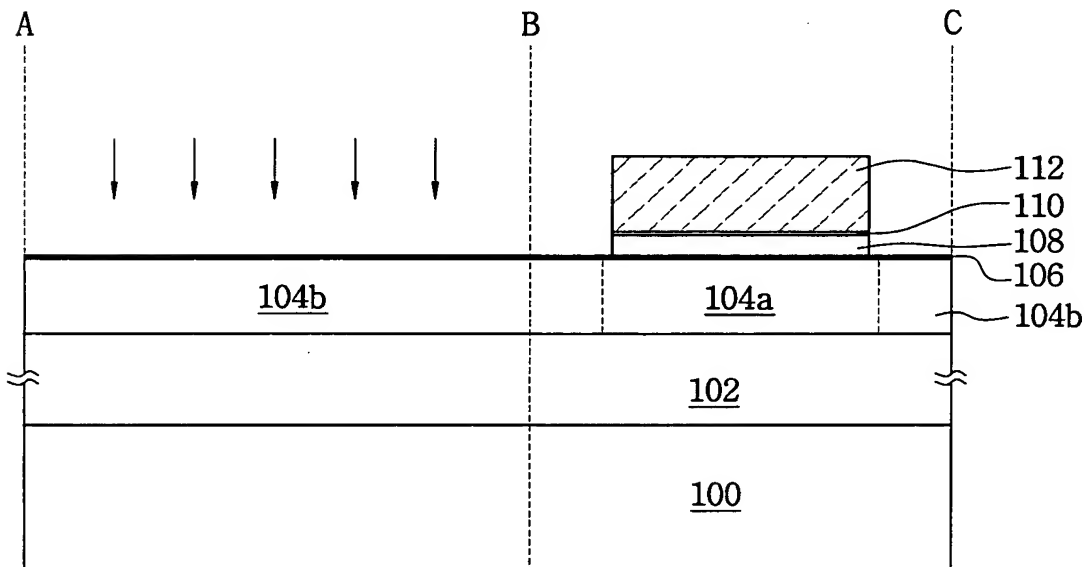


FIG. 4B



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FIG. 4C

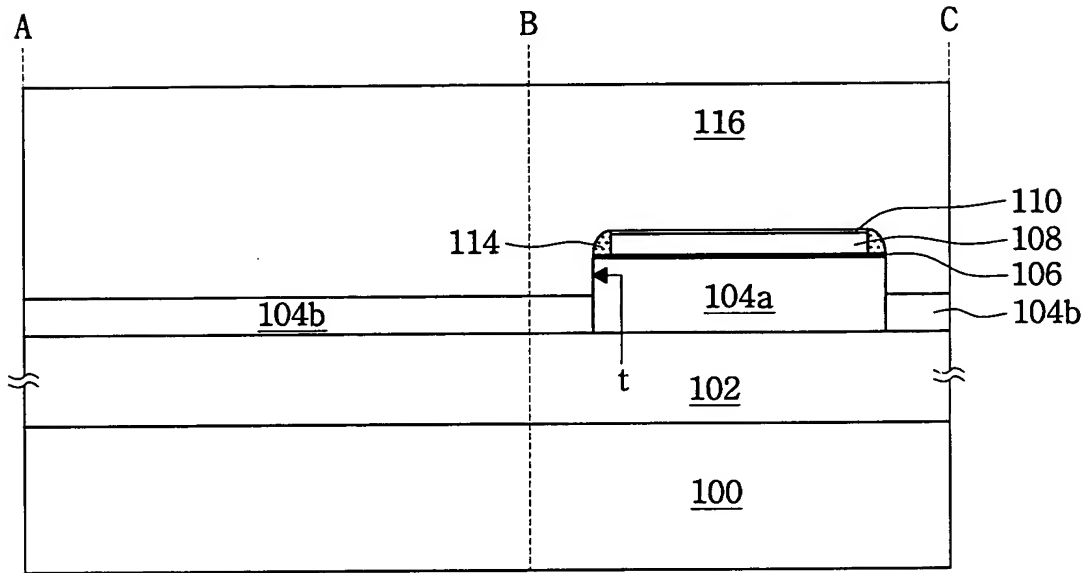
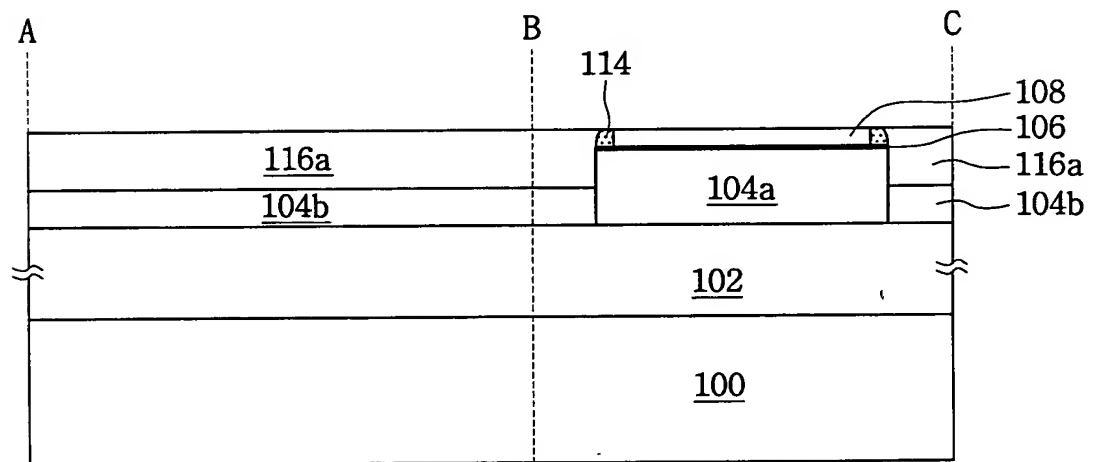


FIG. 4D



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FIG. 4E

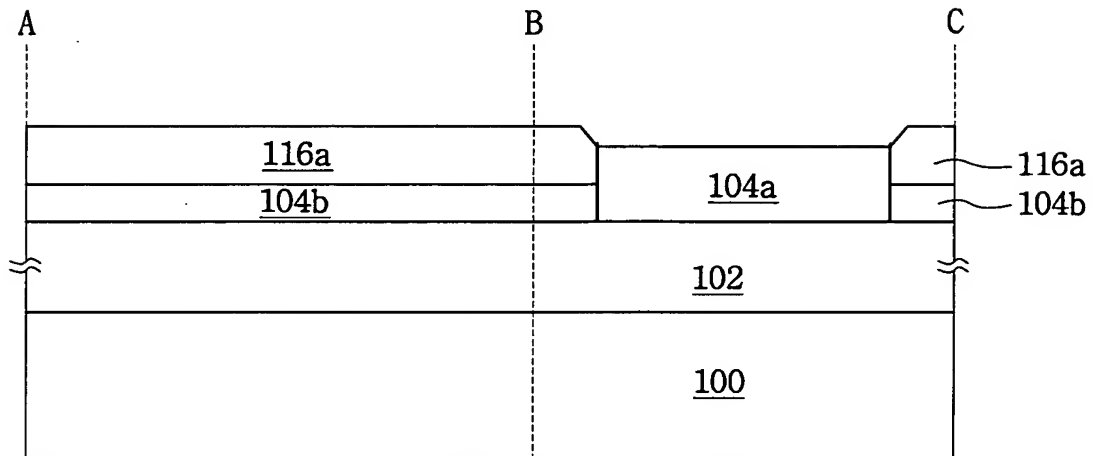
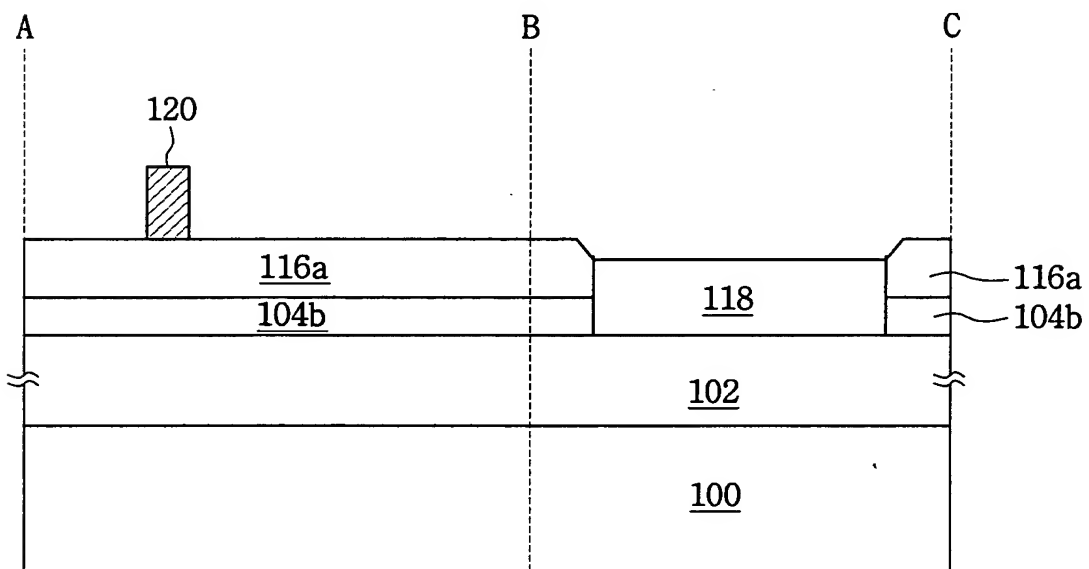


FIG. 4F



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FIG. 4G

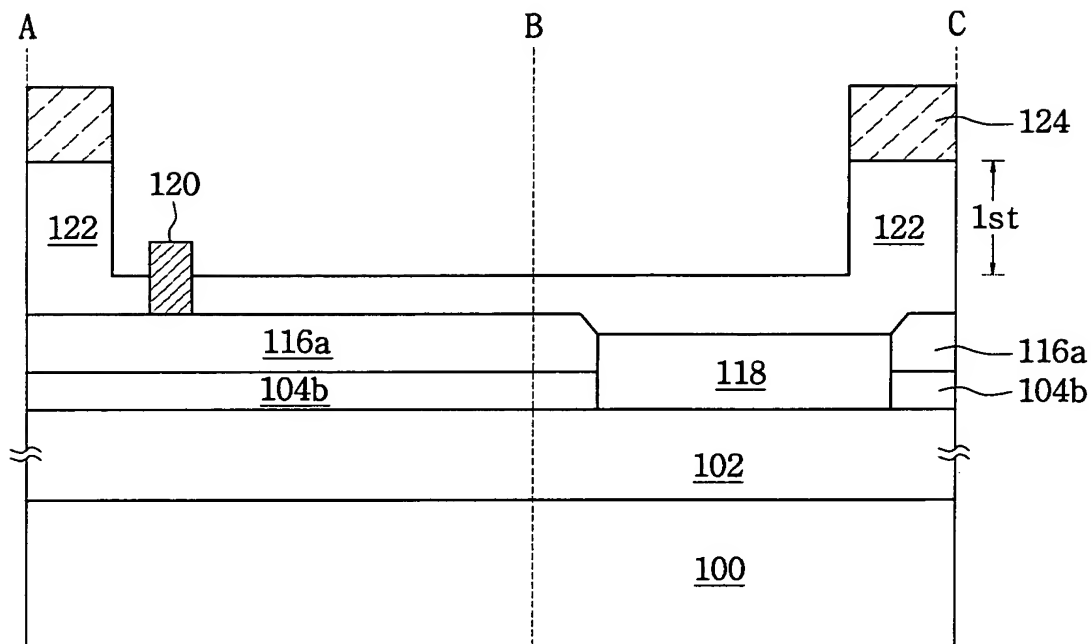
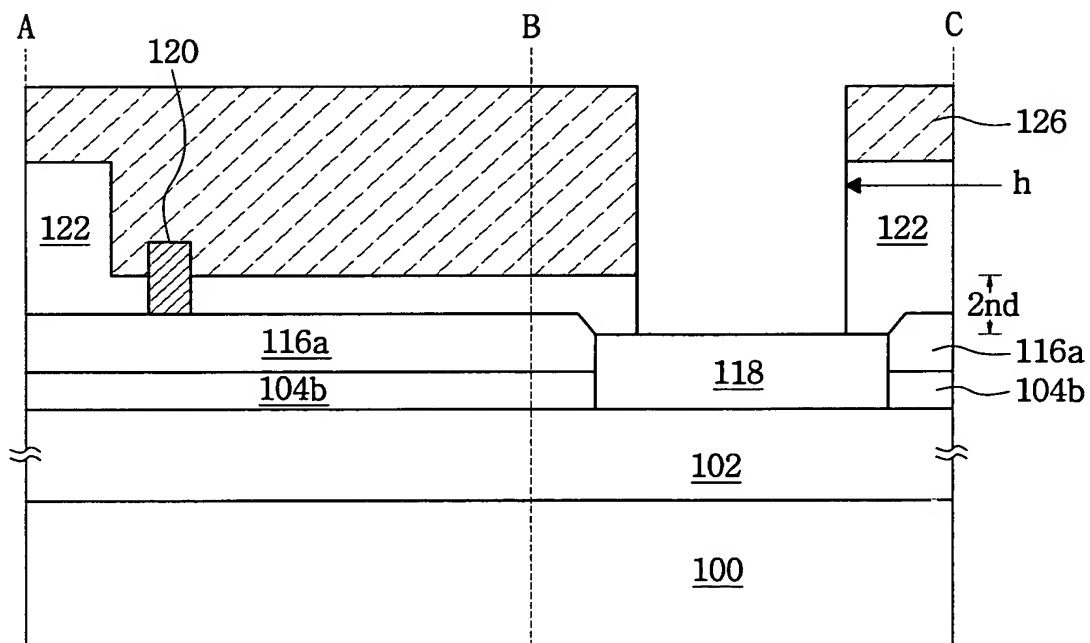


FIG. 4H



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FIG. 4I

